UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,287	09/12/2003	Feng Chen	TI-35766 (032350.B524)	7460

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EXAMINER
WILLIAMS, HOWARD L

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/661,287	CHEN, FENG
	Examiner	Art Unit	
	Howard L. Williams	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *13 September 2004*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12 and 14-17* is/are rejected.

7)☒ Claim(s) *5,13 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

The disclosure is objected to because of the following informalities: The specification does not describe how applicant manipulates the explicitly shown (page 12 lines 9-25) first order transfer function to obtain a second order transfer function. The passive circuit depicted does not provide a third order transfer function, i.e. a first order and a second order ($S * S^2 = S^3$). Additionally, the drawings do not illustrate a third-order filter. Appropriate correction is required. No new matter may be added.

The response states that the objection was not understood. The reference to third order transfer function derives from the multiplicative property of cascaded filters. However, the objection is not based upon this. As stated above:

The specification does not describe how applicant manipulates the explicitly shown (page 12 lines 9-25) first order transfer function to obtain a second order transfer function. The cited portion of the specification reads:

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> Second order filter 26 comprises a second capacitor C_2 and a second resistor R_2 that filter the first filtered signal to yield an integrated signal. According to the illustrated embodiment, second capacitor C_2 and a second resistor R_2 may be directly coupled to integration node C to filter the first filtered signal according to a low-pass response. Second capacitor C_2 and a second resistor R_2 may be selected according to a desired frequency response. According to the illustrated embodiment, second capacitor C_2 and a second resistor R_2 may be selected so that the frequency response substantially approximates a direct current (DC) frequency response. For example, second capacitor C_2 and a second resistor R_2 may be selected according to Equation (2):
>
> $$\frac{1}{R_2 C_2} \approx DC \qquad (2)$$

The statement describing filter 26 as a second order filter is <u>fundamentally incorrect</u>. A single resistor and capacitor do not provide a second order filter. Such a circuit provides a transfer function of 1/sCR (s being representing the Laplace frequency

domain). This is a first order transfer function, i.e. exponent of s = 1. Therefore, the
description does not describe a first order filter and a second order filter from the circuit
that is shown and described.

Claims 1-20 are objected to because of the following informalities: The claimed
passive filter providing a first order and a second order filter is not commensurate with
the description. Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all
obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed
> or described as set forth in section 102 of this title, if the differences between the
> subject matter sought to be patented and the prior art are such that the subject
> matter as a whole would have been obvious at the time the invention was made
> to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was
> made.*

Claims 1-4, 6-12, and 14-17 are rejected under 35 U.S.C. 103(a) as being
unpatentable over the Benabes et al. article (*Passive sigma-delta converter design*) in
view of the Chen et al. article (*A 0.25 mW 13 b passive $\Sigma\Delta$ modulator for a 10 MHz IF
input*) and Yamakido et al. (US 5,227,795) or Voorman et al. (US 5,103,228). Benabes
et al. article *Passive Sigma-Delta Converters Design* discloses a delta-sigma ADC with
a continuous time passive filter (fig. 3 page 471). Benabes et al. also discloses a
discrete time feedback circuit via the DAC shown in figure 1 (page 469). Benabes et al.
shows in figure 2 a model of the feedback loop, input is taken as zero for figure 2,
shown as a switch and hold element which is seen as reasonably suggestive of a
capacitor for the hold element. Chen et al. discloses use of passive filtering delta-sigma
ADC using switched capacitors in the feedback loop. Use of switched capacitor as the
DAC feedback element in Benabes would have been obvious to provide a simple and
compact DAC and the use of RC passive filters would provide reduced switching noise.
Benabes et al. and Chen et al. don't specify whether the respective input signals are a
voltage or a current signal so they don't disclose a transconductance element.
Yamakido et al. and Voorman et al. disclose transconductance elements (V-I) to provide

a current for summing with the fedback signal. The inclusion of a transconductance element in Benabes et al. would have been obvious because current summing is faster and more simply implemented than voltage summing.

Applicant's arguments filed 13 September 2004 have been fully considered but they are not persuasive. Whether the present applicant is the author of the cited (and applied) Chen article is not particularly relevant. The examiner had assumed that it was someone different because surely applicant has cited relevant art of which he/she is aware. Beyond this the response comments to the examiner's clairvoyance. Ahh, if it were so. In reality Benabe's discloses a passive continuous time delta sigma converter that has passive continuous time forward path filter depicted in figure 3. The Chen article provides in figure 2:
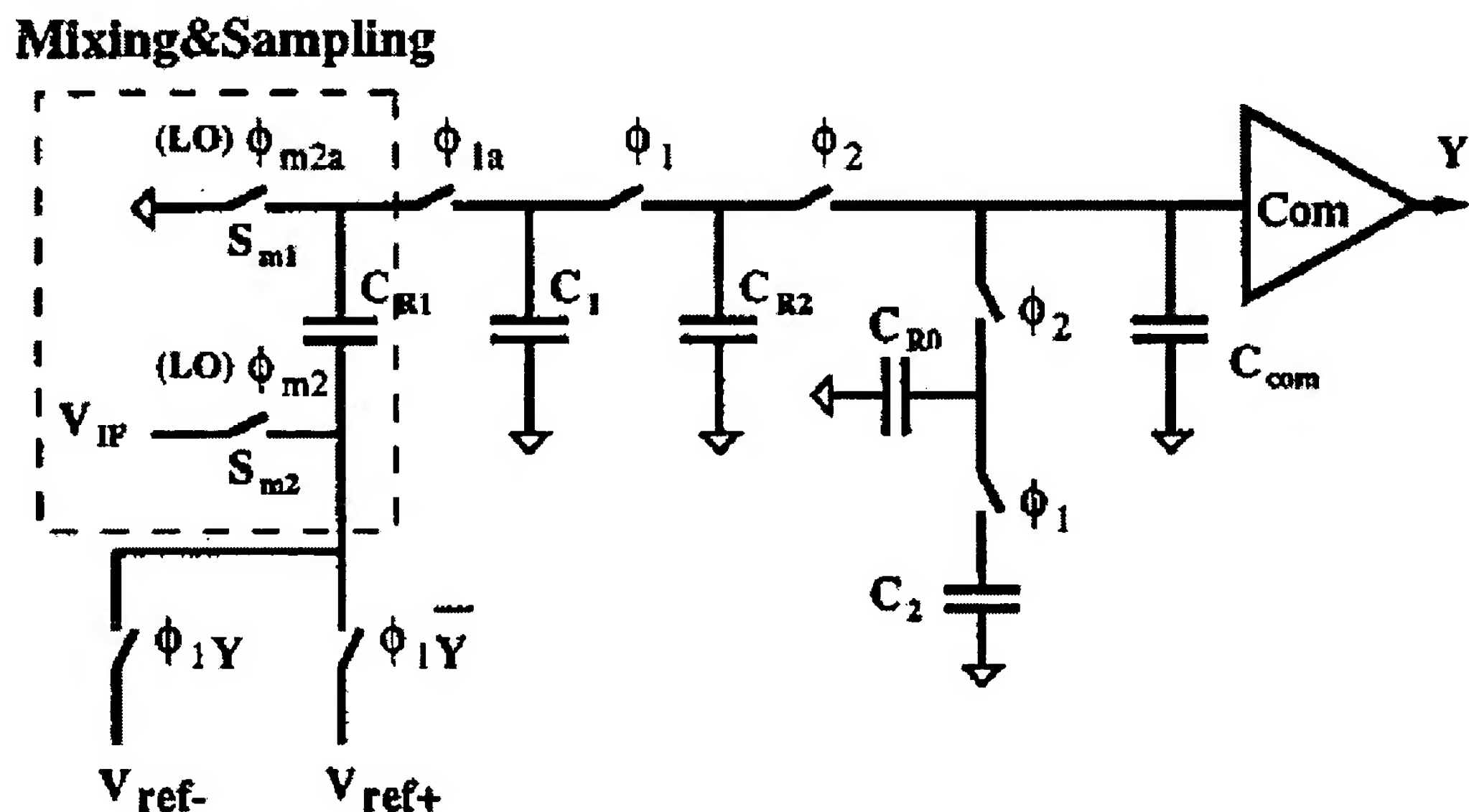
It is also rather interesting that the element C_{R2} and the two switches clocked on Φ_1 and

Φ_2 simulate a resistor as well known in switched capacitor technology. Capacitor C_{R0}

and its two closest switches function likewise. The choice of subscripts for these two

capacitors supports this reading. If one were to redraw the Chen article figure 2 circuit

replacing the capacitors C_{R2}, C_{R0} and the adjacent switches one pretty much gets a

single line figure 2 of the present application. And with no clairvoyance required.

Accordingly the rejection will be maintained.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Claims 5, 13 and 18-20 would be allowable if claims 5, 13 and 18 were rewritten

to overcome the claim objection above.

The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. Vander Zwan et al. (US 6,404,367) and Rich (US 4,860,012)

disclose delta-sigma ADC using continuous time loop filters.

Your Reference: TI-35766 (032350.B524)
Art Unit: 2819

Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571.272.1815. The Patent and Trademark Office has a new central facsimile number for application specific correspondence intended for entry, it is 703-872-9306.

18 November 2004
Voice 571.272.1815

Howard L. Williams
Primary Examiner
Art Unit 2819